OP-44

HIGH-SPEED, PRECISION
OPERATIONAL AMPLIFIER ($A_{VCL} \geq 3$)

Precision Monolithics Inc.

OBSOLETE

FEATURES

- **Slew Rate** ..... **100V/μs Min**
- **Gain-Bandwidth Product** ..... **15MHz Min**
- **Common-Mode Rejection** ..... **86dB Min**
- **Open-Loop Gain** ..... **500V/mV Min**
- **Offset Voltage** ..... **750μV Max**
- **Bias Current** ..... **200pA Max**
- **Excellent AC CMR and PSR**
- **Radiation Hard**

ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99	HERMETIC DIP	LCC	
1.00	OP44AJ*	OP44AZ*	OP44ARC/883*	MIL
0.75	OP44EJ	OP44EZ	—	IND
1.50	OP44FJ	OP44FZ	—	IND

Plastic Mini-Dip and SOIC to be announced.

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

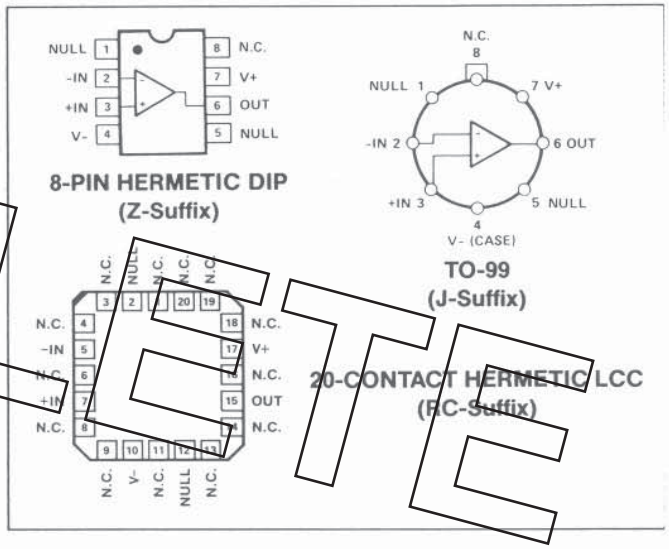
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

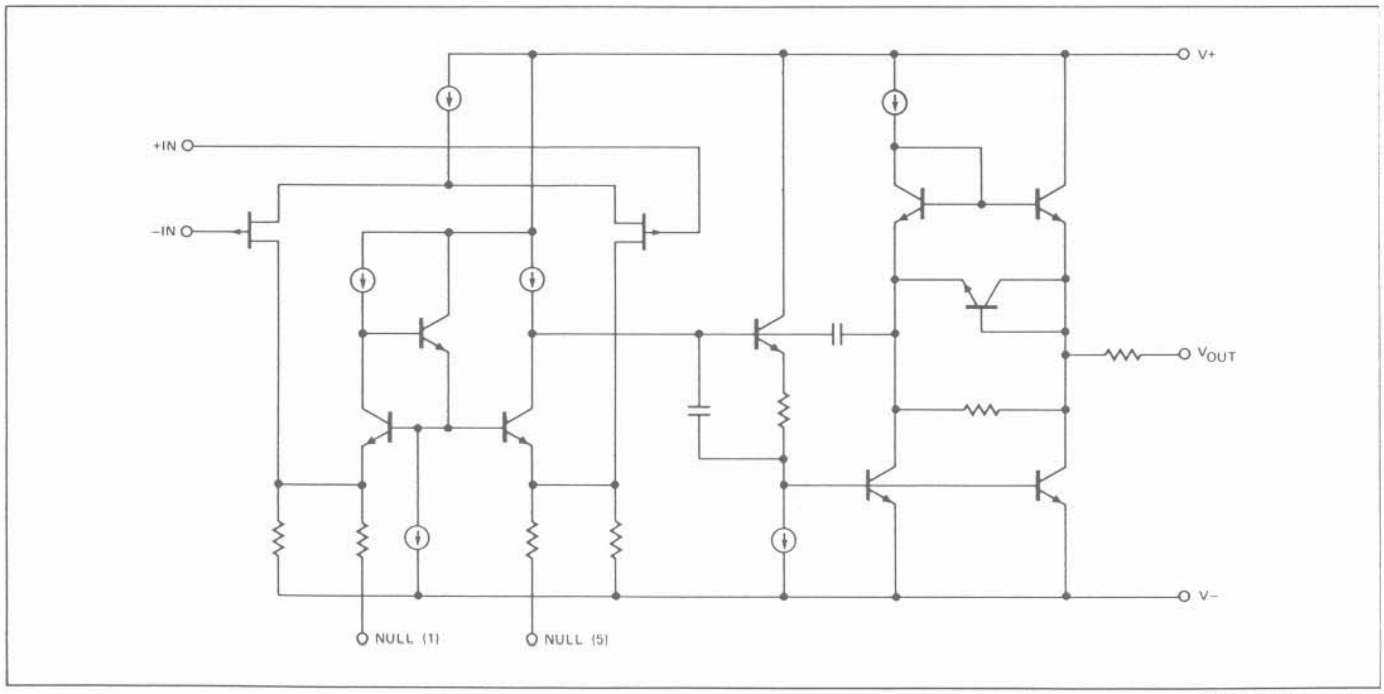
The OP-44 is a fast precision JFET-input operational amplifier delivering a 120V/μs typical slew rate in closed-loop gains of three or more. Full-power bandwidth is 2MHz for a $20V_{p-p}$ sine-wave, and 4MHz for a $10V_{p-p}$ signal. Gain-bandwidth product is typically 23MHz. Settling time to 0.1% is 200ns, and to 12 bits (0.01%) is 800ns, typical. Wideband noise is minimized by only $12nV/\sqrt{Hz}$ flatband noise.

Excellent DC precision makes the OP-44 unique among high-speed amplifiers. Offset voltage below 750μV and 10μV/°C maximum drift eliminates the need for external nulling potentiometers in most applications. Common-mode rejection of 86dB minimum and an open-loop gain of 500V/mV ensures high linearity. Errors due to bias current are virtually eliminated with the OP-44's 200pA maximum input current.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



Applications for the OP-44 include data acquisition systems, pulse amplifiers, RF, IF and video amplifiers, and signal generators.

The OP-44 conforms to the standard 741 pinout with nulling to V−. It offers an excellent upgrade for circuits using the LF400 and AD509. The HA-2520/22/25 are easily upgraded by removing any external nulling components.

For a unity-gain stable amplifier sharing many of the OP-44's characteristics, consult the OP-42 data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±20V
Internal Power Dissipation (Note 3) 500mW
Input Voltage (Note 2) ..... ±20V
Differential Input Voltage (Note 2) 40V
Peak Output Current 50mA
Storage Temperature Range ..... −65°C to 175°C
Operating Temperature Range
OP-44A (J, Z) ..... −55°C to +125°C
OP-44E, F (J, Z) ..... −25°C to +85°C
Junction Temperature ..... −65°C to 175°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than ±20V, the absolute maximum input voltage is equal to the supply voltage.
3. See table for maximum ambient temperature and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
Hermetic 8-Pin DIP (Z)	75°C	6.7mW/°C
Hermetic 20-Contact LCC (RC)	72°C	7.8mW/°C

OBSOLETE

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

			OP-44E			OP-44F			OP-44A			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}		—	0.3	0.75	—	0.4	1.5	—	0.3	1.0	mV
Input Bias Current	I_B	$V_{CM} = 0V$ $T_j = 25°C$	—	80	200	—	130	250	—	80	200	pA
Input Offset Current	I_{OS}	$V_{CM} = 0V$ $T_j = 25°C$	—	4	40	—	6	50	—	4	40	pA
Input Voltage Range	IVR	(Note 1)	±11	+12.5 −12.0	—	±11	+12.5 −12.0	—	±11	+12.5 −12.0	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm11V$	86	96	—	80	92	—	86	96	—	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm10V$ to $\pm20V$	—	9	40	—	12	50	—	9	40	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$ $V_O = \pm10V$ $R_L = 2k\Omega$ $T_j = 25°C$ $R_L = 1k\Omega$	500 200 100	900 260 170	— — —	500 200 100	900 260 170	— — —	500 200 100	900 260 170	— — —	V/mV
Output Voltage Swing	V_O	$R_L = 1k\Omega$	±11.5	+12.5 −11.9	—	±11.5	+12.5 −11.9	—	±11.5	+12.5 −11.9	—	V
Output Current	I_{OUT}		±20	+33 −28	—	±20	+33 −28	—	±20	+33 −28	—	mA
Supply Current	I_{SY}	No Load $V_O = 0V$	—	6.5	7.5	—	6.5	7.5	—	6.5	7.5	mA
Slew Rate	SR	$R_L = 2k\Omega$ $C_L = 50pF$	100	120	—	80	100	—	100	120	—	V/μs
Full-Power Bandwidth	BW_p	$V_O = \pm10V$ (Note 2)	1.5	2.0	—	1.2	1.6	—	1.5	2.0	—	MHz
Gain-Bandwidth Product	GBW	$A_V = 10$ (Note 3)	15	23	—	15	23	—	15	23	—	MHz
Settling Time	t_s	10V Step 0.1% (Note 4)	—	0.2	—	—	0.2	—	—	0.2	—	μs
Rise Time	t_r	$V_O = \pm200mV$ (Note 3, 4)	—	25	50	—	25	50	—	25	50	ns
Overshoot		$V_O = \pm200mV$ (Note 3, 4)	—	25	40	—	25	50	—	25	40	%
Overload Recovery Time	t_{OR}		—	700	—	—	700	—	—	700	—	ns
Capacitive Load Drive Capability	C_L	$A_{VCL} \geq 3$ (Note 3)	50	150	—	50	150	—	50	150	—	pF

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-44E MIN	OP-44E TYP	OP-44E MAX	OP-44F MIN	OP-44F TYP	OP-44F MAX	OP-44A MIN	OP-44A TYP	OP-44A MAX	UNITS
Input Resistance	R_{IN}	(Note 3)	10^8	10^{12}	—	10^8	10^{12}	—	10^8	10^{12}	—	Ω
Open-Loop Output Resistance	R_O		—	50	—	—	50	—	—	50	—	Ω
Voltage Noise	$e_{n\ p-p}$	0.1Hz to 10Hz	—	2	—	—	2	—	—	2	—	μV_{p-p}
Voltage Noise Density	e_n	$f_O = 10Hz$	—	38	—	—	38	—	—	38	—	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	16	—	—	16	—	—	16	—	
		$f_O = 1kHz$	—	13	—	—	13	—	—	13	—	
		$f_O = 10kHz$	—	12	—	—	12	—	—	12	—	
Current Noise Density	i_n	$f_O = 1kHz$	—	0.007	—	—	0.007	—	—	0.007	—	$pA/\sqrt{Hz}$
External V_{OS} Trim Range		$R_{pot} = 10k\Omega$	—	4	—	—	4	—	—	4	—	mV
Long-Term V_{OS} Drift			—	5	—	—	5	—	—	5	—	μV/ month
Supply Voltage Range	V_S	(Note 3)	±8	±15	±20	±8	±15	±20	±8	±15	±20	V

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed by slew-rate test and formula $BW_p = SR/(2\pi 10V_{PEAK})$.
3. Guaranteed but not tested.
4. See test circuit, page 7.

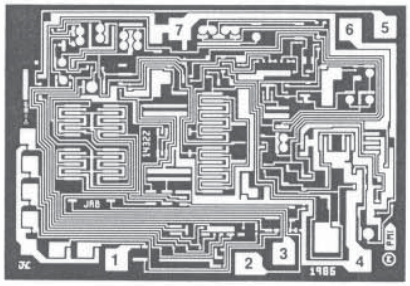
OBSOLETE

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $-25°C \le T_A \le 85°C$ for E/F grades, and $-55°C \le T_A \le 125°C$ for A grade, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-44E MIN	OP-44E TYP	OP-44E MAX	OP-44F MIN	OP-44F TYP	OP-44F MAX	OP-44A MIN	OP-44A TYP	OP-44A MAX	UNITS
Offset Voltage	V_{OS}		—	0.4	1.2	—	0.6	2.5	—	0.5	2.0	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		—	4	10	—	8	—	—	4	10	μV/°C
Input Bias Current	I_B	(Note 1)	—	0.5	1.2	—	0.6	2.0	—	6	20	nA
Input Offset Current	I_{OS}	(Note 1)	—	0.05	0.2	—	0.06	0.4	—	0.2	1.0	nA
Input Voltage Range	IVR	(Note 2)	±11	+12.5 −12.0	—	±11	+12.5 −12.0	—	±11	+12.5 −12.0	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm11V$	84	94	—	80	92	—	84	94	—	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm10V$ to ±20V	—	2	40	—	6	50	—	10	50	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$ (Note 1)	200	500	—	200	500	—	160	350	—	V/mV
		$R_L = 2k\Omega$ $V_O = \pm10V$	100	160	—	100	160	—	80	110	—	
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±11.0	+12.3 −11.8	—	±11.0	+12.3 −11.8	—	±11.0	+12.3 −11.8	—	V
Output Current	I_{OUT}		±8	—	—	±8	—	—	±8	—	—	mA
Supply Current	I_{SY}	No Load $V_O = 0V$	—	6.5	7.5	—	6.5	7.5	—	6.5	7.5	mA
Slew Rate	SR	$R_L = 2k\Omega$; $C_L = 50pF$	80	100	—	70	90	—	80	100	—	V/μs
Capacitive Load Drive Capability	C_L	$A_{VCL} \ge 3$ (Note 3)	50	100	—	50	100	—	50	100	—	pF

NOTES:
1. $T_j = 85°C$ for E/F Grades; $T_j = 125°C$ for A grade.
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

DICE CHARACTERISTICS



DIE SIZE 0.098 × 0.070 inch, 6860 sq. mils
(2.49 × 1.78 mm, 4.43 sq. mm)

1. OFFSET VOLTAGE NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. NEGATIVE SUPPLY
5. OFFSET VOLTAGE NULL
6. AMPLIFIER OUTPUT
7. POSITIVE SUPPLY

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

OBSOLETE

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_j = 25°C$, unless otherwise noted.

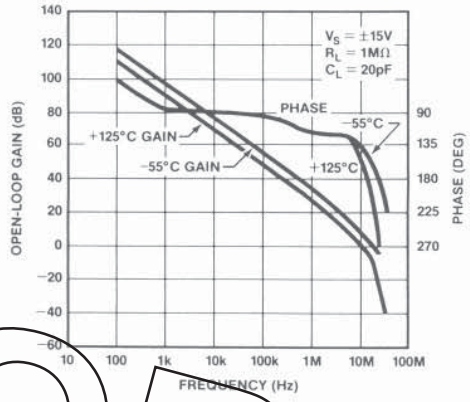
PARAMETER	SYMBOL	CONDITIONS	OP-44N LIMIT	UNITS
Offset Voltage	V_{OS}		1.5	mV MAX
Input Bias Current	I_B	$V_{CM} = 0V$	250	pA MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	50	pA MAX
Input Voltage Range	IVR	(Note 1)	±11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	90	dB MIN
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	50	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$ $R_L = 2k\Omega$ $R_L = 1k\Omega$	500 200 100	V/mV MIN
Output Voltage Swing	V_O	$R_L = 1k\Omega$	±11.5	V MIN
Output Current	I_{OUT}		±20	mA MIN
Supply Current	I_{SY}	No Load $V_O = 0V$	7.5	mA MAX
Slew Rate	SR		80	V/μs MIN
Capacitive Load Drive Capability	C_L	$A_{VCL} \geq 3$ (Note 2)	50	pF MIN

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed but not tested.

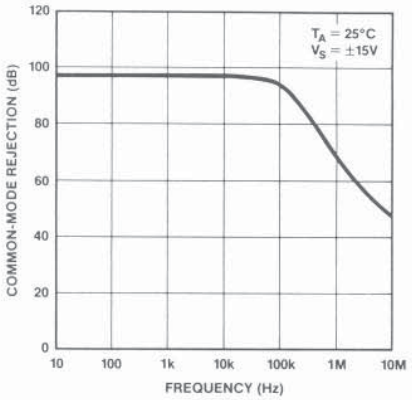
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

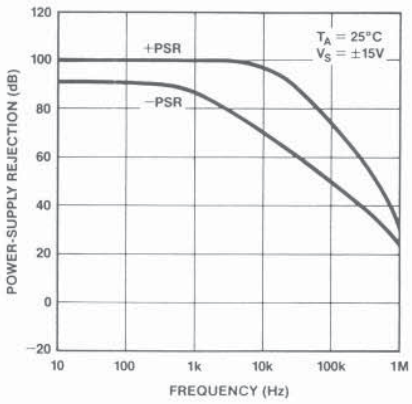
OPEN-LOOP GAIN, PHASE vs FREQUENCY



COMMON-MODE REJECTION vs FREQUENCY

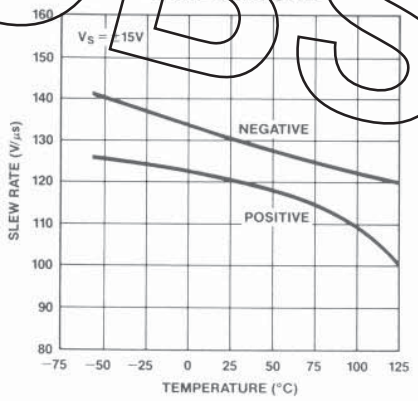


POWER-SUPPLY REJECTION vs FREQUENCY

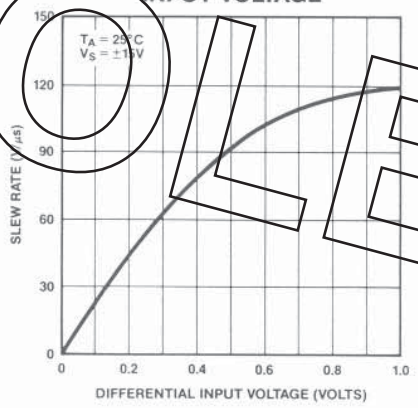


OBSOLETE

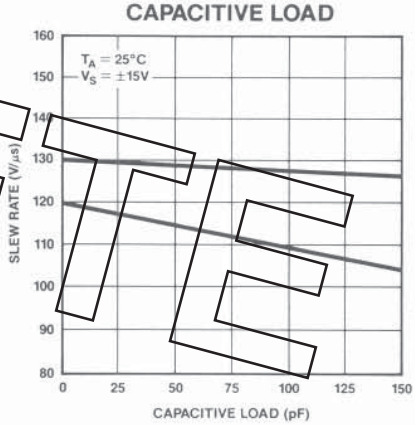
SLEW RATE vs TEMPERATURE



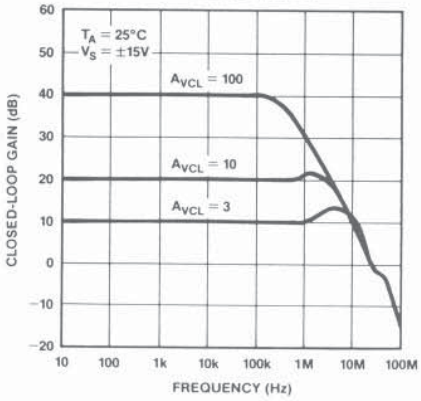
SLEW RATE vs DIFFERENTIAL INPUT VOLTAGE



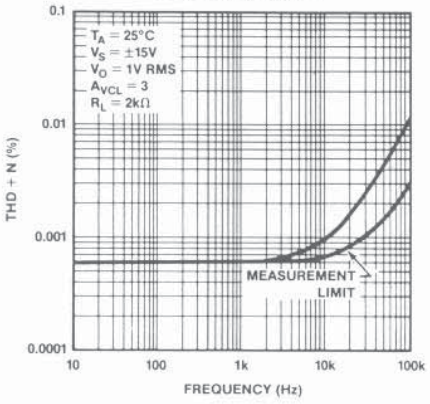
SLEW RATE vs CAPACITIVE LOAD



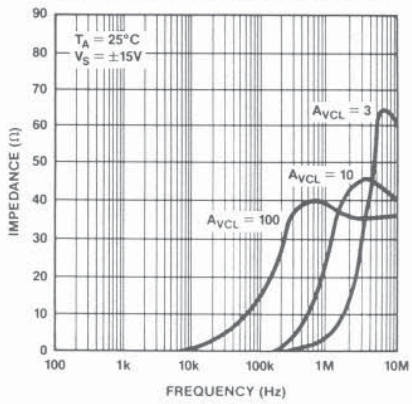
CLOSED-LOOP GAIN vs FREQUENCY



TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

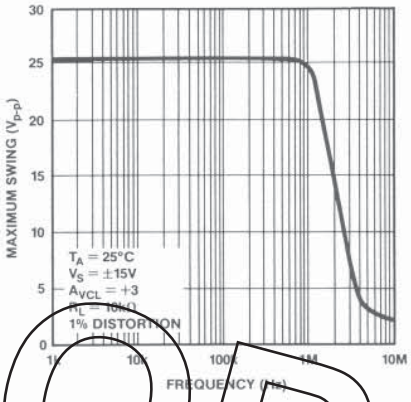


CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

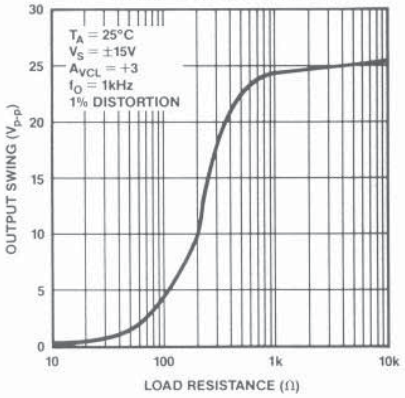


TYPICAL PERFORMANCE CHARACTERISTICS

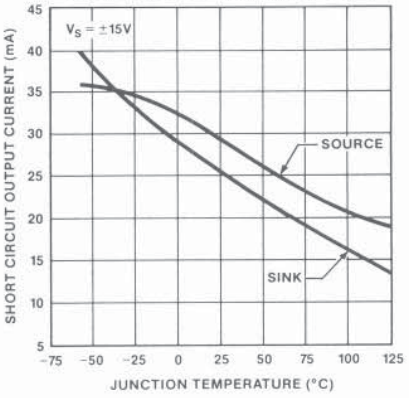
MAXIMUM OUTPUT SWING vs FREQUENCY



OUTPUT SWING vs LOAD RESISTANCE

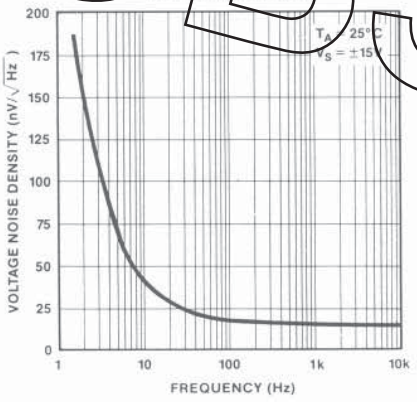


SHORT CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE

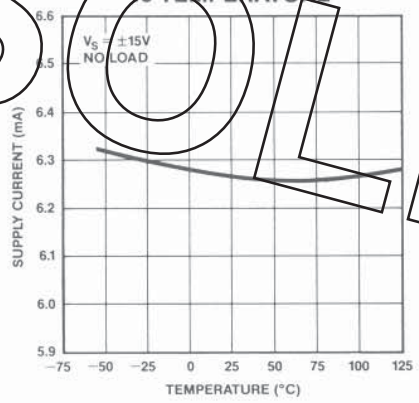


OBSOLETE

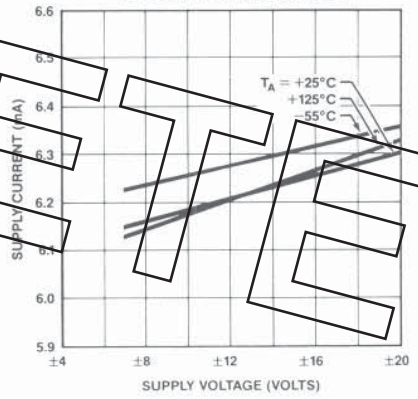
VOLTAGE NOISE DENSITY vs FREQUENCY



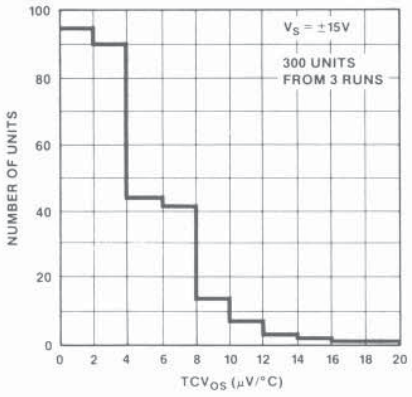
SUPPLY CURRENT vs TEMPERATURE



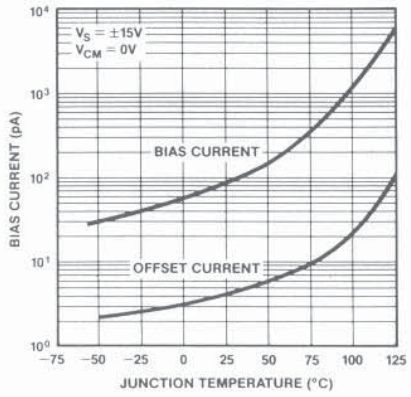
SUPPLY CURRENT vs SUPPLY VOLTAGE



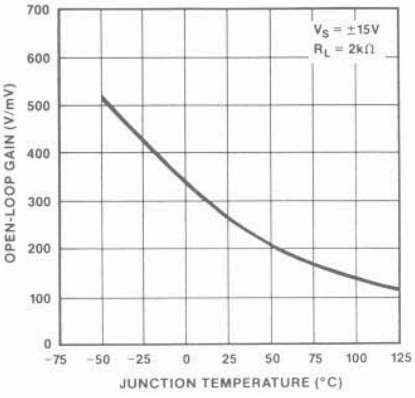
TYPICAL DISTRIBUTION OF TCV_{OS}



BIAS, OFFSET CURRENT vs JUNCTION TEMPERATURE



OPEN-LOOP GAIN vs JUNCTION TEMPERATURE



APPLICATIONS INFORMATION

The OP-44 is a high-speed amplifier internally compensated for closed-loop gains of 3 or more. Slew rate is typically 120V/μs, which allows the OP-44 output to handle a $20V_{p-p}$ sine wave at 2MHz. Stability is ensured by the OP-44's guaranteed capacitive load drive ability of 50pF.

The input capacitance of high-speed op amps often causes a noticeable degradation of pulse response, resulting in excessive overshoot and ringing. The pole introduced by the input capacitance can be compensated by placing a similar capacitance in the feedback loop of the amplifier. For the OP-44, the input capacitance is typically 6pF.

Small-signal and large-signal transient responses are shown in Figures 1 and 2. These photos were taken using the gain of 3 test circuit shown in Figure 3.

As with most JFET-input op amps, the output of the OP-44 may undergo phase inversion if either input exceeds the specified input voltage range. Phase inversion will not damage the amplifier, nor will it cause an internal latch-up.

FIGURE 1: Small Signal Transient Response ($A_{VCL} = +3$, $C_L = 50pF$)

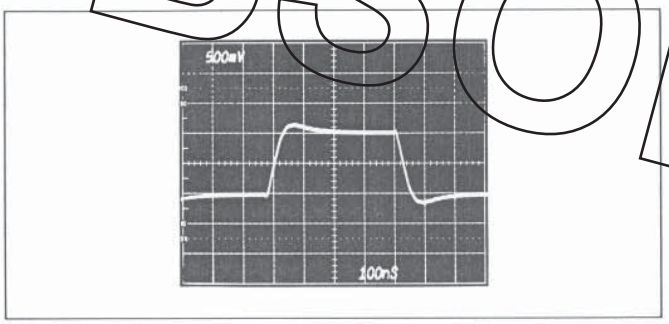
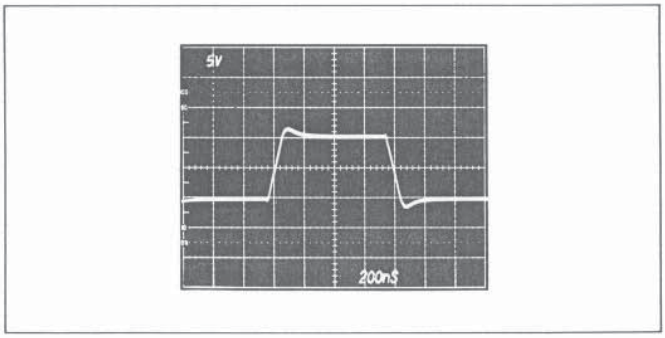


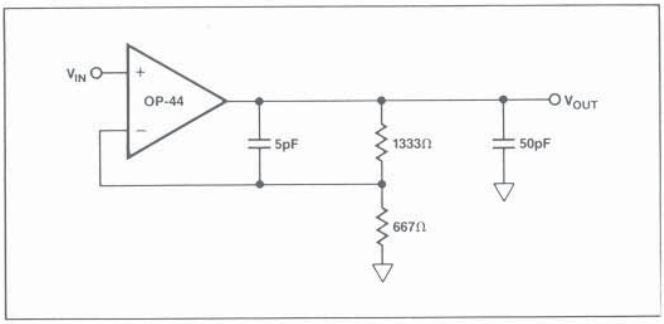
FIGURE 2: Large-Signal Transient Response ($A_{VCL} = +3$, $C_L = 50pF$)



Supply decoupling must be used to overcome inductance and resistance associated with the supply lines to the amplifier. For most applications, a 0.1μF to 0.01μF placed between each supply pin and ground is adequate. If supply lines are extremely long and/or noisy, an additional tantalum capacitor between 3.3μF and 10μF should be placed in parallel with each of the smaller decoupling capacitors.

The OP-44 displays excellent resistance to radiation. Radiation hardness data is available by contacting the factory.

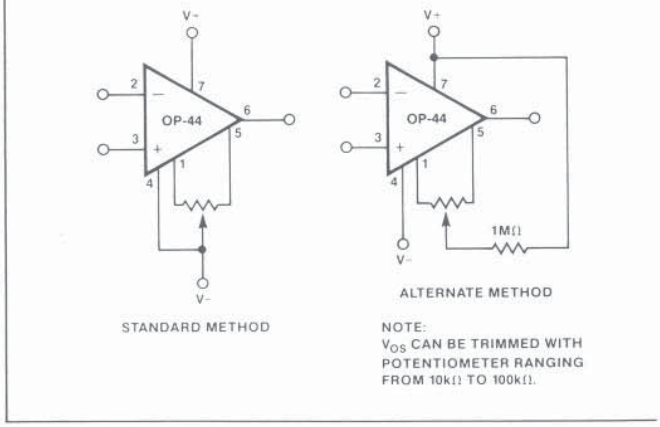
FIGURE 3: Transient Response Test Circuit



OFFSET VOLTAGE ADJUSTMENT

Offset voltage is adjusted with a 10kΩ to 100kΩ potentiometer as shown in Figure 4. The potentiometer is connected between pins 1 and 5 with its wiper connected to the V– supply. Nulling V_{OS} in this manner changes TCV_{OS} by no more than 5μV/°C per millivolt of V_{OS} change. Alternately, V_{OS} may be nulled by attaching the potentiometer wiper through a 1MΩ resistor to the positive supply rail.

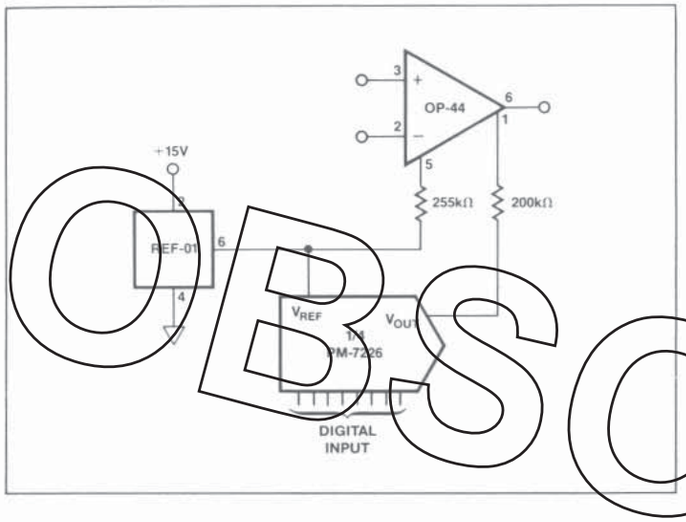
FIGURE 4: Input Offset Voltage Nulling



OBSOLETE

Digital offset correction is possible using the nulling pins. The circuit of Figure 5 will correct for greater than ±4mV of offset, allowing correction of some system errors in addition to the OP-44's offset voltage. One of the four voltage-output DACs on the PM-7226 is used to apply a voltage between 0V and 10V to the 200kΩ resistor, while the 255kΩ resistor is tied to the +10V reference. One LSB of the 8-bit PM-7226 is equivalent to approximately 35μV of offset change around the zero offset point.

FIGURE 5: Digital Offset Correction



A common problem with many high-speed amplifiers is a requirement for more DC precision than the amplifier's capability. While the OP-44 already offers an order of magnitude or more improvements in precision over previous high-speed amplifiers, some users may find a need for even greater precision.

Figure 6 shows a combination amplifier melding the precision DC characteristics of an OP-97 with the high speed of the OP-44. The OP-97 reacts for low-frequency and DC signals, while the OP-44 is dominant at higher frequencies. Overcompensation of the OP-97 ensures that it operates only at low frequencies. Resistor matching is important to optimize this circuit's transient response. The overall supply current of this combination amplifier is only slightly higher than that of the OP-44 alone. This is due to the minimal consumption of the OP-97, only 600μA. Transient response of this circuit is shown in Figure 7. Its initial offset voltage is 20μV, while TCV_{OS} is less than 0.6μV/°C.

FIGURE 6: High-Speed, Low-Offset, Low-Drift Amplifier

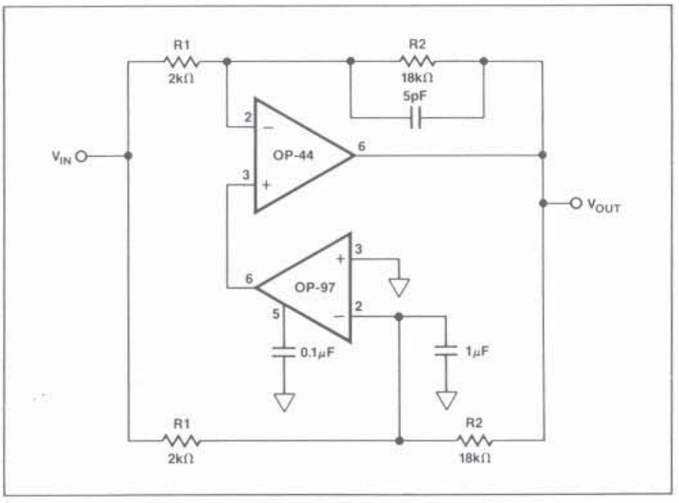


FIGURE 7: Combination Amplifier Transient Response

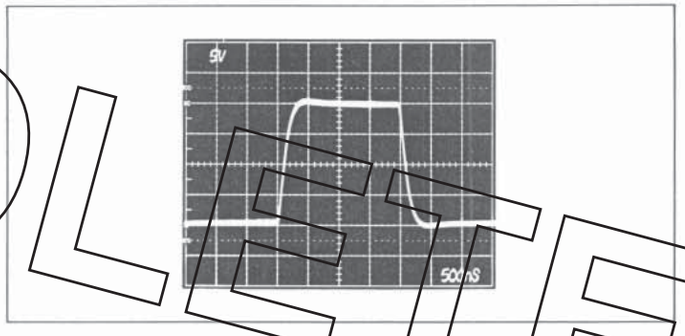
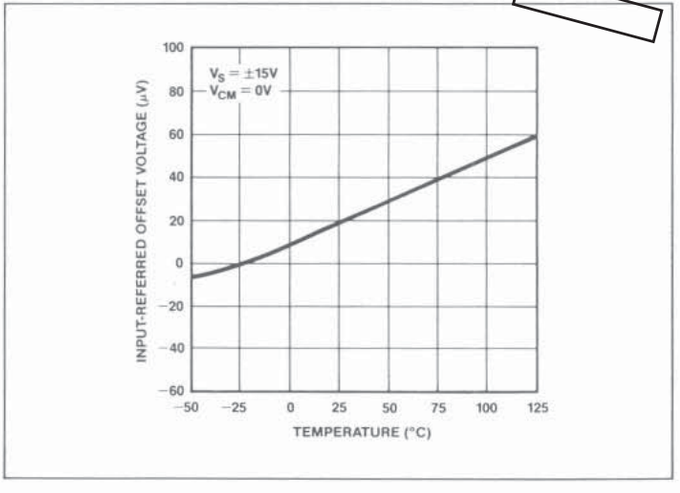
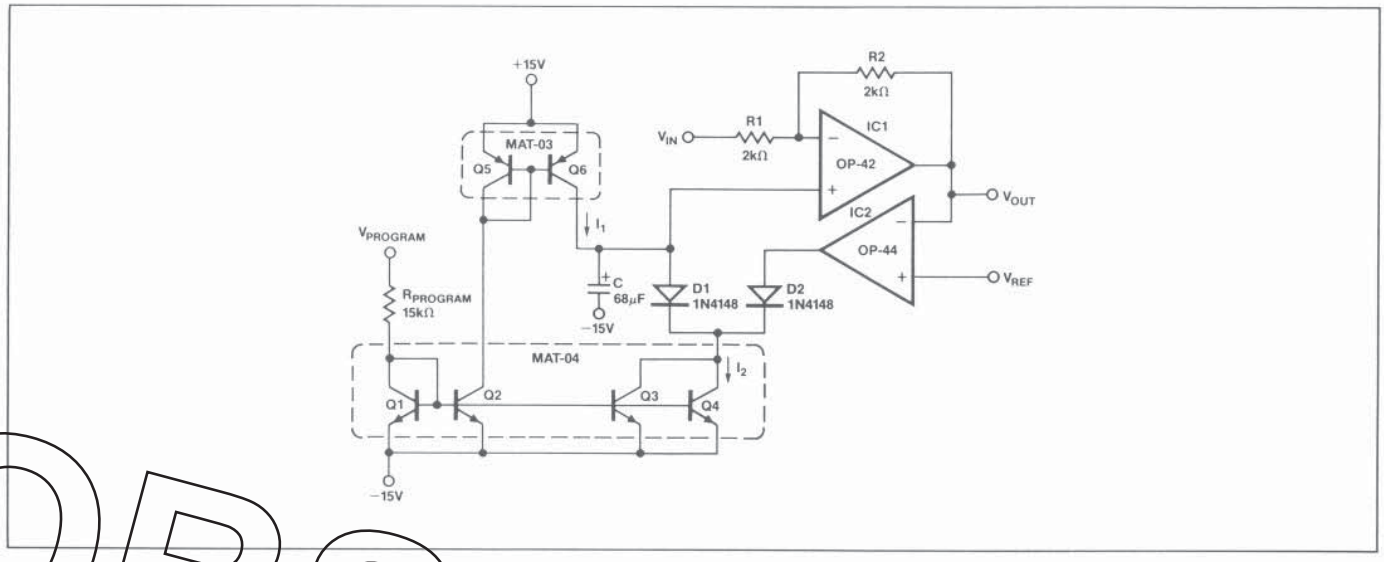


FIGURE 8: Combination Amplifier V_{OS} vs Temperature



OBSOLETE

FIGURE 9: Programmable Baseline Restorer



OBSOLETE

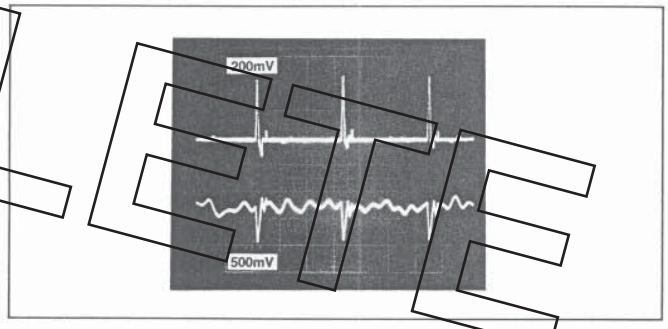
Baseline restoration is another useful technique for correcting errors introduced by amplifier drift, or by electromagnetic pickup. High-impedance sources, such as a human body, are notorious for large DC drifts. In many cases, where pulse or AC measurements are being made, and the pulse height above a nominal DC line contains the important information.

While a simple high-pass filter may be adequate for some situations, the baseline restorer shown in Figure 9 allows a wide degree of flexibility for analog adaptive filtering techniques, and offers some benefits not available with a frequency-domain filter.

The baseline restorer behaves as a nonlinear filter, acting upon the slew rate of the input signal rather than its frequency. Its output will restore the base of the pulses to an arbitrary level, set by V_{REF}. The slew rate cutoff of the filter is set by the current flowing through Q1, which is in turn set by $V_{PROGRAM}$. V_{REF} and $V_{PROGRAM}$ may be controlled by a voltage-output DAC such as the PM-7226. If current programming is desired, $R_{PROGRAM}$ may be removed and replaced by a current-source, such as a bipolar DAC.

To understand the circuit's operation, assume that capacitor C has charged to the DC baseline. If the output swings above the baseline, IC2 swings low, reverse biasing diode D2. D1 is pulled low, and forward biases. A current (I_2 - I_1) discharges the capacitor until equilibrium is restored. If the output drops below the baseline, IC2 swings high, and D2 becomes forward biased. I_2 is supplied by the output of IC2 while I_1 charges C until the baseline is restored. The rate of restoration depends upon the current available to charge or discharge C.

FIGURE 10: Baseline Restorer Response



For symmetric operation, with the same restoration rate for positive or negative excursions from the baseline, I_2 must be twice I_1. This provides an equal current for charging and discharging the capacitor. I_1 is set by the current flowing through Q1 in the MAT-04. An identical current flows through each transistor. The MAT-03 matched PNP pair, Q5 and Q6, act as a current mirror to reflect the current through Q2 (I_1). Q3 and Q4 create I_2, which is twice I_1. I_1 may be set anywhere between a few nanoamps to several mA. Higher currents will result in rejection of faster-slewing signals, while lower currents will allow passage of slower signals.

The OP-44 is configured for a gain of −1, but gain is adjustable by R1 and R2, and is simply −(R2/R1). OP-44 stability is maintained by the dominant pole introduced by C.