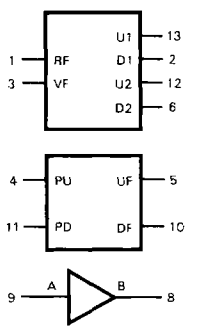
11C44

PHASE/FREQUENCY DETECTOR

11C00 SERIES

GENERAL DESCRIPTION — The 11C44 contains a Phase/Frequency Detector, a Phase Dectector, a Charge Pump, and an Amplifier. The Phase/Frequency Detector accepts TTL signals representing a Reference Frequency (RF) and a Variable Frequency (VF), compares the relative timing of their negative going transitions, and generates either and UP (U1) or a DOWN (D1) signal whose duration is equal to the RF-VF timing difference. When the RF and VF signals have the same frequency, the Phase Detector outputs U2 and D2 provide binary signals whose duty cycles are proportional to the phase angle between RF and VF. The Charge Pump can be driven from U1 and D1 or U2 and D2, and has three possible output states representing CHARGE, DISCHARGE, and HOLD instructions when applied to an integrator. The Amplifier is a Darlington transistor with grounded emitter and uncommitted collector and base. The 11C44 thus contains several of the functional elements used in phase-locked loop applications. It is pin compatible with the Motorola MC4044/4344, but has better discrimination capability for small phase differences.

LOGIC SYMBOL

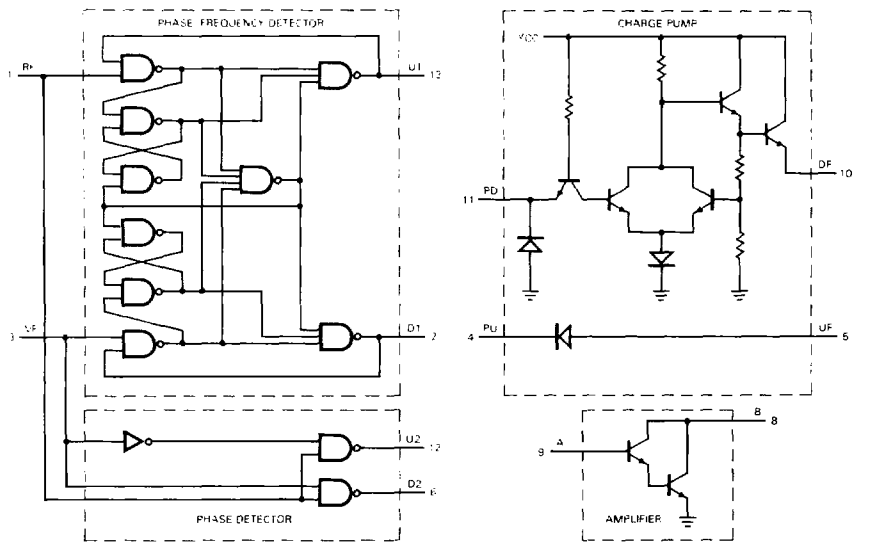


V_{CC} = Pin 14
GND = Pin 7

FUNCTIONS

RF — Reference Frequency Input
VF — Variable Frequency Input
U1, D1 — Phase/Frequency Detector Outputs
U2, D2 — Phase Detector Outputs
PU, PD — Charge Pump Inputs
UF, DF — Charge Pump Outputs
A — Amplifier Input
B — Amplifier Output

LOGIC DIAGRAM AND SCHEMATIC



RECOMMENDED OPERATING CONDITIONS

PART NUMBER	SUPPLY VOLTAGE V_{dc}		AMBIENT TEMPERATURE °C	
	MIN	MAX	MIN	MAX
11C44DC — Commercial	4.75	5.25	0	+75
11C44DM — Military	4.5	5.5	-55	+125

DC CHARACTERISTICS: (over operating temperature range unless otherwise noted)

SYMBOL	CHARACTERISTIC	PIN(s)	LIMITS B	LIMITS A	UNITS	CONDITIONS		V_{CC1}
V_{IH}	Input HIGH Voltage	1, 3, 11	2.0		V	Per Truth Tables		MIN
V_{IL}	Input LOW Voltage	1, 3, 11		0.9	V	Per Truth Tables		MIN
V_{OH2}	Output HIGH Voltage	2, 6, 12, 13	2.4		V	11C44DM	I_{OH} = -1.6 mA	MIN
			2.5		V	11C44DC		
V_{OL2}	Output LOW Voltage	2, 6, 12, 13		0.5	V	I_{OL} = 20 mA		MIN
V_{CD}	Clamp Diode Voltage	1, 3, 11	-1.5		V	I_{IN} = -10 mA; T_A = 25°C only		MIN
I_{IL}	Input LOW Current	1, 3	-4.8		mA	V_{IN} = 0.4 V		MAX
		11	-1.6					
I_{IH}	Input HIGH Current	1, 3		120	µA	V_{IN} = V_{OH} MIN		MAX
		11		40				
		1, 3, 11		1.0	mA	V_{IN} = 5.5 V; T_A = 25°C only		MAX
I_{CEX2}	Output Leakage Current	2, 6, 12, 13		250	µA	V_{OUT} = 5.0 V		5.0 V
I_{SC2}	Short-circuit Output Current	2, 6, 12, 13	-65	-20	mA	V_{OUT} = 0 V		5.0 V
V_{EH}	Output HIGH Voltage	10	1.5		V	I_{OH} = -1 mA; Pin 11 = V_{IL}		MIN
I_{ER}	Output Leakage Current	10		5.0	µA	Pin 10 = 1.5 V; Pin 11 = V_{OH} MIN		MAX
I_C	Amplifier Output Current	8	1.0		mA	T_A = MAX	I_B Pin 9 = 2 µA V_{CE} Pin 8 = $V_{CC(MAX)}$	MAX
			0.8		mA	T_A = 25°C		
			0.5		mA	T_A = 0°C;11C44DC		
			0.2		mA	T_A = -55°C;11C44DM		
I_{CES}	Amplifier Leakage Current	8		120	µA	Pin 9 = gnd; V_{CE} Pin 8 = $V_{CC(MAX)}$		MAX
V_{FD}	Diode Forward Voltage	5	0.5		V	I_{FD} Pin 5 = 1 mA; Pin 4 = gnd		5.0 V
I_{RD}	Diode Reverse Current	4		5.0	µA	V_R Pin 4 = 5.5 V; Pin 5 = gnd		5.0 V
I_{CC}	Power Supply Current	14		40	mA	Inputs Open		5.0 V

NOTES:
1. Min and Max refer to the recommended Vcc values for the particular device type.
2. Apply voltage or current sources to outputs only after outputs are in the appropriate states.
Outputs 2 and 13 require sequential RF-VF exercising to assure proper states.

TESTING — Testing the Phase/Frequency Detector requires some preliminary exercising of RF and VF to get U1 and D1 into predictable states. Any number of sequences can be devised from the flow table in *Figure 5. Figure 1* shows a sequence that contains all possible combinations of input, output, and internal states. This sequence can also be used cyclically, as suggested by the double designations of the last three steps, which makes it useful for the type of functional testing that requires repetitive output waveforms.

For parametric testing, which is normally much more time consuming than functional testing, it may be desirable to use a short sequence to minimize overall test time. In parametric testing, the act of disconnecting a forcing function from U1 or D1 often creates an electrical disturbance in the wiring and cabling, which in turn triggers the Phase/Frequency Detector into another state. It is therefore recommended that the inputs be resequenced between successive tests. *Figure 2* lists short sequences that get the outputs into the three possible combinations.

RF and VF should be sequenced in Grey code to avoid ambiguities due to timing differences in the RF-VF signal sources. Depending on the noise characteristics of the test apparatus, it is advisable to use RF-VF input signal levels considerably above the listed V_{IH} and below the V_{IL} levels. For an I_{SC} test, the RF-VF inputs should be in the O-O state to avoid retriggering through the internal feedback when U1 or D1 is forced to zero volts. Input sequencing is not required for testing U2 and D2. The truth table for the Phase Detector is shown in *Figure 3.*

STEP #	INPUTS		OUTPUTS	
	RF	VF	U1	D1
1	1	0	X	X
2	0	0	X	X
3	1	0	X	X
4	0	0	0	1
5	1	0	0	1
6	1	1	0	1
7	0	1	0	1
8	0	0	1	1
9	0	1	1	1
10	0	0	1	0
11	0	1	1	0
12	1	1	1	0
13	1	0	1	0
14	0	0	1	1
15	1	0	1	1
16	1	1	1	1
17/1	1	0	1	0
18/2	0	0	1	1
19/3	1	0	1	1

X = Undefined

Fig. 1 Cyclical Sequence for Phase/Frequency Detector Testing

STEP #	INPUTS		OUTPUTS	
	RF	VF	U1	D1
1a	1	0	X	X
2a	0	0	X	X
3a	1	0	X	X
4a	0	0	0	1
1b	1	1	X	X
2b	0	1	X	X
3b	0	0	X	X
4b	0	1	X	X
5b	0	0	1	0
1c	1	1	X	X
2c	1	0	X	X
3c	1	1	X	X
4c	1	0	X	X
5c	0	0	1	1

X = Undefined

Fig. 2 Short Sequences for Phase/Frequency Detector Testing

INPUTS		OUTPUTS	
RF	VF	U2	D2
0	0	1	1
0	1	1	1
1	0	0	1
1	1	1	0

Fig. 3 Phase Detector Truth Table

FUNCTIONAL DESCRIPTION — 11C44 operation is best explained by examining its role in a typical application, such as the phase-locked loop shown in the block diagram of *Figure 4*. In this arrangement a relatively low frequency oscillator is made to control a much higher frequency VCO. The ÷ N counter scales down the VCO output frequency (OF) and provides a variable frequency (VF) in the same range as the reference frequency (RF). For example, with RF of 100 kHz and OF of 120 MHz, the counter is set to divide by 1200. External controls such as thumbwheel switches are used to change the counter divide ratio, which in turn leads to a change in OF. Extending the foregoing example, changing the counter modules from 1200 to 1201 effectively reduces VF below 100 kHz. The detector generates an error signal which ultimately increases the VCO frequency until VF again equals RF at 100 kHz. The net result is that OF is increased to N x RF, in this case 120.1 MHz. The loop also corrects for VCO drift, since a change in OF causes VF to be higher or lower than RF, in turn causing the detector to generate a corrective signal and pull the VCO back into lock.

Phase detection can be performed by simple functions such as a latch or an Exclusive-OR, but these are susceptible to locking on harmonics. To avoid this effect, a detector must ignore repetitive state changes on one of its inputs unless and until a state change occurs on the other input. This requires internal memory. The 11C44 Phase/Frequency Detector contains several internal latches, as can be seen in the logic diagram. When power is first applied, the circuit can settle in any one of several states for any combination of RF and VF input states. Subsequent response to RF and VF transitions can be predicted from the sequential flow table of *Figure 5*.

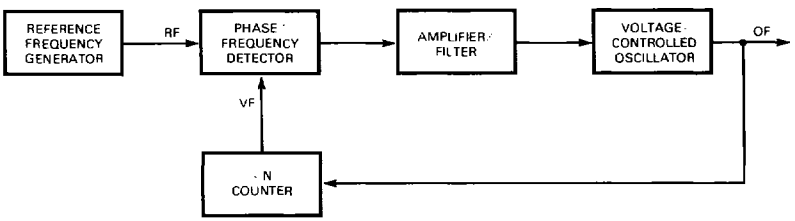


Fig. 4 General Arrangement for Phase-Locked Loop

Each possible combination of RF, VF, U1 and D1 is identified by a number in the flow table. If the number is in parenthesis, it indicates a stable state; without parenthesis it indicates an unstable state. Note that for any given combination of RF-VF inputs, *i.e.*, in each column, there are three possible stable states corresponding to the three possible combinations of U1 and D1. To determine the circuit response to an input change, first move horizontally from the column representing the present input combination to the column representing the new input combination. This will identify the new state number. If this new state number is not in parenthesis, move vertically to the same number in parenthesis. For example, if the RF-VF input combination changes from 1-1, with the circuit in state (7), to 1-0, move right to state 12. Since this is an unstable state, move down to (12). This is the new state of the circuit and is the starting point for determining circuit response to a subsequent input change.

The flow table shows that if the inputs change back and forth between 0-0 and 1-1, the circuit changes state accordingly between (5) and (7), while U1 and D1 remain in the 1-1 condition. Note that when RF-VF changes back and forth repeatedly between 0-0 and 1-1, it means that the two inputs agree both in phase and frequency. Thus the constant 1-1 signals from U1 and D1 indicate the LOCK condition. *Figures 6* and *7* show how U1 and D1 respond when RF and VF differ in frequency or phase. State numbers correspond to stable states in the flow table. In *Figure 6a*, VF is lower in frequency than RF, causing a periodic LOW signal from U1 and a constant HIGH from D1. The U1 signal indicates that the VCO frequency should be increased. In *Figure 6b*, VF is higher than RF, causing a periodic LOW signal from D1 and a constant HIGH from U1. The D1 signal means that the VCO frequency should be decreased.

Figures 7a and *7b* show that the Phase/Frequency Detector can respond in either of two ways to the same set of RF and VF inputs, if they differ in phase but have the same frequency. In *Figure 7a*, the circuit is assumed to start in state (2); the result is a signal at U1 whose duration in the LOW state is 50% of a full cycle time, indicating that VF lags RF by 180°. In *Figure 7b*, the circuit is assumed to start in state (6), leading to a D1 signal whose LOW duration is 50% of a full cycle time. This indicates that VF leads RF by 180°, which is, of course, the same as saying that VF lags RF by 180°. Thus the output indications of *7a* and *7b* are equivalent. Other supplementary lead/lag angle indications can also occur, such as 90° lead/270° lag, 120° lead/240° lag, etc. These situations are not likely to arise in any operating loop but can easily occur in bench tests using a pair of slaved pulse generators for RF and VF signal sources and momentarily interrupting V_{CC} to the detector.

RF-VF INPUT STATES				OUTPUTS	
0-0	0-1	1-1	1-0	U1	D1
(1) 5	2 (2)	3 (3)	(4) 8	0 0	1 1
(5) 9	6 (6)	7 7	8 1 2	1 1	1 1
5 1	2 2	(7) 7	12 (8)	1 1	1 1
(9) 5	(10) 6	11 (11)	12 (12)	1 1	0 0

Fig. 5 Flow Table for Phase/Frequency Detector

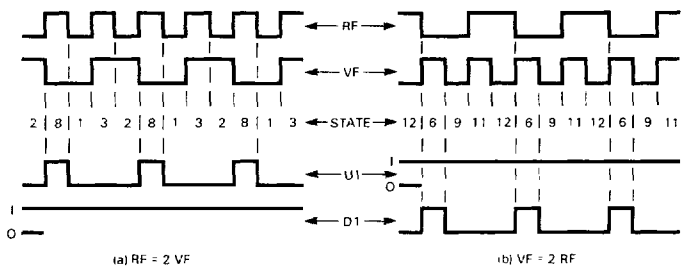


Fig. 6 Phase/Frequency Detector Response for Unequal Input Frequencies

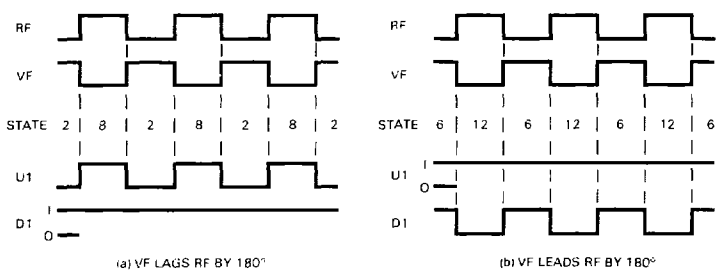


Fig. 7 Alternate Interpretations by the Phase/Frequency Detector

FUNCTIONAL DESCRIPTION (Cont.)
The Charge Pump consists of a diode connected between terminals PU and UF, and a special inverter between terminals PD and DF. The inverter output has only a pull-up transistor. Thus when DF is HIGH, it is a low impedance source with an output voltage of about +2.25 V. When the PD input goes HIGH, the base of the DF pull-up transistor is held near ground potential and thus the DF output is a very high impedance. With the Charge Pump driven from the Phase/Frequency Detector as indicated in *Figure 8*, a LOW signal at the PU input causes the UF output to be a low impedance to ground, with an output voltage of approximately +0.75 V. When the PU input is HIGH, the diode is back biased and is thus a high impedance. For symmetric phase detector gain in the pump-up and pump-down modes, the effective input threshold of the amplifier, symbolized as V_{REF} in *Figure 8*, should be midway between the UF level of +0.75 and the DF level of +2.25 V, or about +1.5 V.

Figure 9 shows an arrangement for evaluating detector output as a function of phase difference between RF and VF. The internal delay controls of the pulse generators provide phase angle variations approaching ±360°, limited somewhat by the tendency of a pulse generator to become erratic when the internal delay approaches the pulse period. With the generator outputs in phase, the Charge Pump produces no output pulses and the measured voltage is +1.5 V. Dealying the output of a generator A with respect to B causes the Charge Pump to produce positive pulses extending to +2.25 V. The pulse duration is equal to the time between the negative edge of B and the negative edge of A. As the delay is increased toward a full cycle (360°), the filtered output approaches +2.25 V. Conversely, delaying the output of generator B with respect to A causes the Charge Pump to produce negative pulses extending down to +0.75 V. The pulse duration equals the delay from the negative edge of A to the negative edge of B; as the delay approaches 360°, the filtered output approaches +0.75 V. Plotting the output voltage as a function of lead or lag angle gives the characteristic shown in *Figure 10*. The slope of the characteristic, and thus the detector gain, is approximately 0.12 V/radian.

The variation of detector gain in the vicinity of zero phase difference is of particular interest to system designers. Finite internal delays limit the ability of the Phase/Frequency Detector to respond to small differences in timing between the negative edges of RF and VF. This causes a dead zone in the middle of the characteristic, which can be seen in the expanded graph of *Figure 11*. Immediately to either side of this dead zone the detector gain is greater than average. This effect is also due to internal detector responses involving some of the unstable states shown in the flow table *(Figure 5)* and the internal race conditions which accompany them. The logic circuitry of the 11C44 Phase/Frequency Detector is designed with careful attention to internal switch points, time constants, and path delays. This results in much less severe gain variations than exhibited by the MC4044, as indicated in *Figure 11*.

The Phase Detector has no internal storage, thus the U2-D2 output signals are strictly a function of the present state of RF-VF. From the truth table of *Figure 3*, it can be seen that if the RF and VF input signals have the same frequency and phase, *i.e.*, switch back and forth between 1-1 and 0-0, the U2 output is always HIGH and the D2 output has a 50% duty cycle. If the RF-VF signals switch between 0-1 and 1-0 (180° out of phase), D2 will remain HIGH and the U2 output will exhibit a 50% duty cycle. For any other phase angle between RF and VF, U2 and D2 will each be active (LOW) during some part of an input cycle. For a 90° phase angle between RF and VF, U2 and D2 will each exhibit a 25% (LOW) duty cycle.

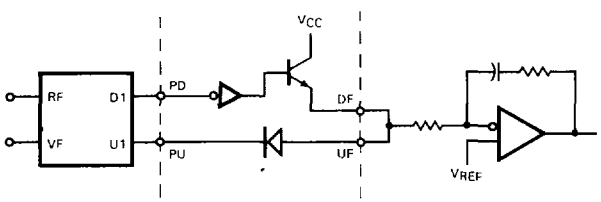
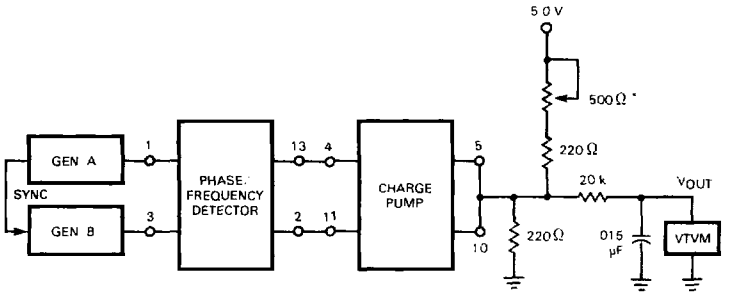


Fig. 8 Charge Pump Connections



*Adjust for V_{OUT} = 1.5 V with D.U.T. unplugged.

Fig. 9 Phase/Frequency Detector Gain Test

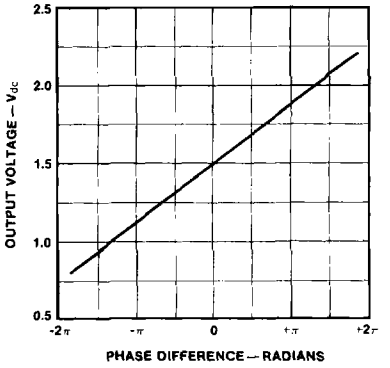


Fig. 10 Output Voltage vs Phase Difference

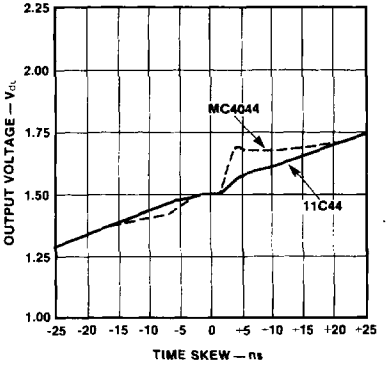
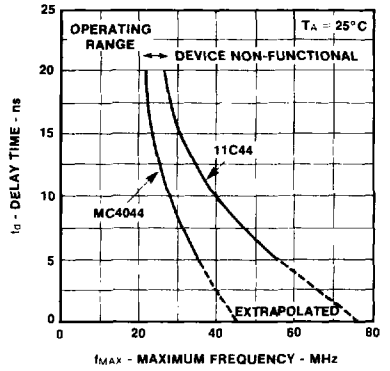
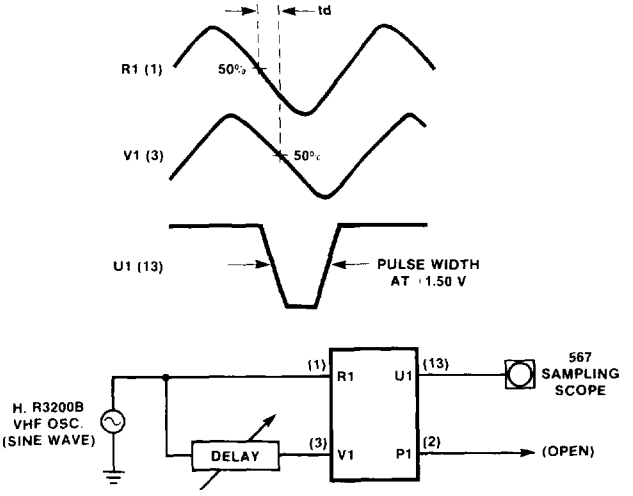


Fig. 11 Detector Output Response Near Lock





DELAY TIME VS MAXIMUM FREQUENCY